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Gordon Edward Morrison et al.

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XAMINER INITIAL		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE IF APPROPRIATE
EE	AA	3 34 3 13 5	9-19-57	Freiman, et al.	340	172.5	
EE	AB	3 61 1 30 6	10-5-71	Reigel	340	172.5	
EE	AC	3 77 1 14 1	11-6-73	Culler	340	172.5	
EE	AD	4 10 4 72 0	8-1-78	Gruner	364	200	
EE	AE	4 10 9 31 1	8-22-78	Blum, et al.	364	200	
EE	AF	4 15 3 93 2	5-8-79	Dennis, et al.	364	200	
EE	AG	4 18 1 93 6	1-1-80	Kober	364	200	
EE	AH	4 22 8 49 5	10-14-80	Bernhard	364	101	
EE	AI	4 22 9 79 0	10-21-80	Gilliland, et al.	364	200	
EE	AJ	4 24 1 39 8	12-23-80	Caril	364	200	
EE	AK	4 27 0 16 7	5-26-81	Koehler, et al.	364	200	

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EE	AR	Dennis, "Data Flow Supercomputers", Computer, November, 1980, Pgs. 48-56
EE	AS	Hagiwara, H. et al., "A Dynamically Microprogrammable, Local Host Computer With Low-Level Parallelism", IEEE Transactions on Computers, C-29, N. 7, July, 1980, Pgs. 577-594.
EE	AT	Fisher et al., "Microcode Compaction: Looking Backward and Looking Forward", National Computer Conference, 1981, Pgs. 93-102.

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EC	DA	4 43 5 75 8	3-6-84	Lorie, et al.	364	200	
EC	BB	4 46 8 73 6	8-28-84	DeSantis	364	200	
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EC	BR	Fisher et al., "Using an Oracle to Measure Potential Parallelism in Single Instruction Stream Programs", IEEE No. 0194-1893/81/0000/0171 14th Annual Microprogramming Workshop, Sigmicro, October, 1981, Pgs. 171-182.
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EC	BS	J.R. Vanaken et al., "The Expression Processor, IEEE Transactions on Computers, C-30, No. 8, August, 1981, Pgs. 525-536.

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CS XX	Davis, "Computer Architecture", IEEE Spectrum, November, 1983, Pgs. 94-99.
CT XX	Hagiwara, H. et al., "A User-Microprogrammable Local Host Computer With Low-Level Parallelism", Article, Association for Computing Machinery, #0149-7111/83/0000/0151, 1983, Pgs. 151-157.

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<i>ee</i>	DR XX	McDowell, Charles Edward, "SIMAC: A Multiple ALU Computer", Dissertation Thesis, University of California, San Diego, 1983 (111 pages).
	DS XX	McDowell, Charles E., "A Simple Architecture for Low Level Parallelism", Proceedings of 1983 International Conference on Parallel Processing, Pgs. 472-477.
<i>ee</i>	DT XX	Requa, et al., "The Piecewise Data Flow Architecture: Architectural Concepts, IEEE Transactions on Computers, Vol. C-32, No. 5, May, 1983, Pgs. 425-438.
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EE	ER XX	Fisher, A.T., "The VLIW Machine: A Multiprocessor for Compiling Scientific Code", Computer, 1984, Pgs. 45-52.
EE	ES XX	Fisher, et al., "Measuring the Parallelism Available for Very Long Instruction, Word Architectures", IEEE Transactions on Computers, Vol. C-33, No. 11, November, 1984, Pgs. 968-976.
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